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Improved interfacial and electrical properties of GaAs metal-oxide-semiconductor capacitors with HfTiON as gate dielectric and TaON as passivation interlayer

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The interfacial and electrical properties of sputtered HfTiON on sulfur-passivated GaAs with or without TaON as interfacial passivation layer (IPL) are investigated. Experimental results show that the GaAs metal-oxide-semiconductor capacitor with HfTiON/TaON stacked gate dielectric annealed at 600 °C exhibits low interface-state density ($1.0 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$), small gate leakage current ($7.3 \times 10^{-5} \text{ A cm}^{-2}$ at $V_g = V_{fb} + 1 \text{ V}$), small capacitance equivalent thickness (1.65 nm), and large equivalent dielectric constant (26.2). The involved mechanisms lie in the fact that the TaON IPL can effectively block the diffusions of Hf, Ti, and O towards GaAs surface and suppress the formation of interfacial As-As bonds, Ga-/As-oxides, thus unpinning the Fermi level at the TaON/GaAs interface and improving the interface quality and electrical properties of the device. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4818000>]

GaAs-based metal-oxide-semiconductor field-effect transistor (MOSFET) with high-k gate dielectric has received significant efforts in the past decades due to its higher carrier mobility, larger energy bandgap, and lower power consumption than those of its Si counterpart.^{1,2} However, direct deposition of high-k dielectric on GaAs yields poor electrical characteristics due to easy formation of native oxide on the GaAs surface which results in an extremely high density of interface states, thus inducing Fermi-level pinning at the GaAs/high-k interface.³ So, different surface-passivation techniques of GaAs have been intensively studied. For instance, depositing a thin layer of Si or Ge before deposition of high-k dielectric has been demonstrated to be effective in improving the interface quality.⁴⁻⁶ However, Si or Ge can alter the doping concentration or even induce a counter doping in the GaAs substrate because they are amphoteric dopant for GaAs.⁷ Al₂O₃ or AlON as interfacial passivation layer (IPL) also provides excellent interface quality in GaAs MOS devices,^{8,9} but their low k value (~ 8 for Al₂O₃ and ~ 10 for AlON) limits further device scaling. Ta-based oxynitride (TaON) with a high-k value (~ 26) close to that of HfO₂ has been used as the interlayer of Hf-based Ge MOS devices, which have showed excellent electrical properties.¹⁰ Also, TaON has a large bandgap ($\sim 4.4 \text{ eV}$) and high thermal stability, and so is a promising candidate as IPL on GaAs. In this work, surface pretreatments including sulfur passivation by (NH₄)₂S and especially TaON as IPL are adopted to improve the interface quality of GaAs MOS device with a very high-k HfTiON gate dielectric, and thus excellent electrical properties have been achieved with small gate leakage

current and low interface-state density as compared to its counterpart without the TaON IPL.

MOS capacitors were fabricated on Si-doped n-GaAs (100) wafers with a doping concentration of $0.5 \sim 1.0 \times 10^{18} \text{ cm}^{-3}$. The wafers were degreased in acetone, ethanol, and isopropanol, and dipped in diluted HCl to remove the native oxide, followed by (NH₄)₂S dipping for 40 min at room temperature for sulfur passivation of the GaAs surface and then drying by N₂. Subsequently, a thin TaN layer of $\sim 2 \text{ nm}$ was deposited on the wafers as IPL by reactive sputtering of a Ta target in an Ar/N₂ (24 sccm/12 sccm) ambient, and then a $\sim 8 \text{ nm}$ HfTiN film was *in situ* deposited by co-sputtering of Hf and Ti targets in the same ambient (denoted as HfTiON/TaON sample). For comparison, a control sample with only HfTiN ($\sim 10 \text{ nm}$) as gate dielectric was prepared (denoted as HfTiON sample). Post-deposition annealing (PDA) was performed at 500 °C or 600 °C for 60 s in N₂ (500 sccm) to transform HfTiN/TaN into HfTiON/TaON by using the residual oxygen in the annealing system. Al was thermally evaporated and patterned as gate electrode and also as the back electrode to decrease contact resistance. Finally, the samples were annealed at 300 °C for 20 min in forming gas (5% H₂ + 95% N₂).

High-frequency (HF, 1-MHz) capacitance-voltage (C-V) and gate leakage characteristics (J_g vs. V_g) of the samples were measured using HP4284A precision Laboratoire Central de Recherche meter and HP4156A precision semiconductor parameter analyzer, respectively. High-resolution transmission electron microscopy (HR-TEM) was used to observe the cross-section of the HfTiON/TaON stacked gate dielectric. X-ray photoelectron spectroscopy (XPS) was used to analyze the chemical states at/near the high-k/GaAs interface. Physical thickness of the gate dielectric was determined by ellipsometer and HR-TEM.

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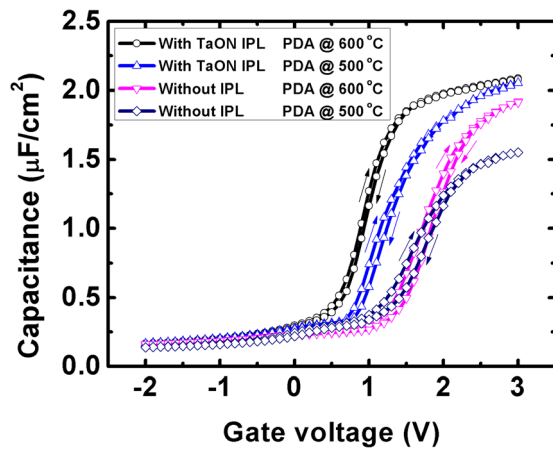


FIG. 1. HF (1-MHz) C-V characteristics of GaAs MOS capacitors with/without TaON, annealed at 500 and 600 °C.

Fig. 1 is the typical HF C-V curve of the samples. For the sample without TaON IPL, a stretch out of the C-V curve is obviously observed, indicating a high density of defective states at the conduction-band edge of GaAs caused by a considerable amount of As-O, As-As, and Ga-O bonds at the GaAs/HfTiON interface.^{11–13} However, the stretch out is diminished for the two HfTiON/TaON samples, and even disappears for the one annealed at 600 °C, which should be ascribed to the blocking role of TaON against oxygen diffusion from the HfTiON gate dielectric to the surface of the GaAs substrate, similar to the works in Refs. 14 and 15. The thin interface layer of TaON (2.6 nm) is observed between HfTiON (8.2 nm) and GaAs, as shown in Fig. 2, and the total physical thickness (T_{ox}) of the stacked gate dielectric is basically consistent with the measured result by ellipsometry (11.1 nm). So, T_{ox} 's of the other samples were also measured by ellipsometry, as listed in Table I. In addition, from Fig. 1, it can be seen that the accumulation capacitance is larger for the HfTiON/TaON sample than the HfTiON sample under the same annealing temperature, although the physical thicknesses of their dielectric films are approximately equal. This indicates that the TaON IPL can efficiently suppress the growth of Ga-/As-oxides and thus a low-k interfacial layer on the GaAs substrate.¹⁶ The larger accumulation capacitance for the HfTiON/TaON sample annealed at 600 °C than that annealed at 500 °C is because better interface quality can be obtained at higher annealing temperature. The quasi-saturation of the C-V curve in the accumulation regime and a large slope in the depletion regime for the HfTiON/TaON sample annealed at

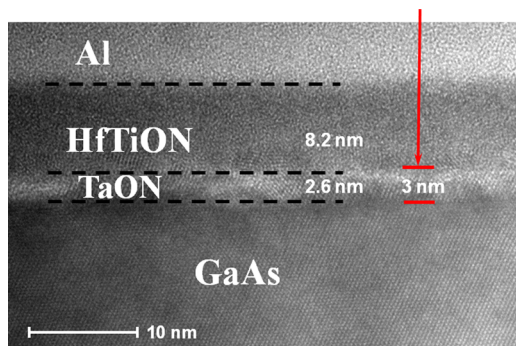


FIG. 2. The cross-sectional HR-TEM image of Al/HfTiON/TaON/GaAs annealed at 600 °C.

TABLE I. Parameters of the GaAs MOS capacitors extracted from HF C-V curves.

Sample	V_{fb} (V)	T_{ox} (nm)	Q_{ox} (cm ⁻²)	D_{it} (cm ⁻² eV ⁻¹)	CET (nm)	k
HfTiON/TaON 600 °C	0.93	11.1	-9.3×10^{12}	1.0×10^{12}	1.65	26.2
HfTiON/TaON 500 °C	1.19	11.2	-1.3×10^{13}	3.8×10^{12}	1.69	25.9
HfTiON 600 °C	1.67	11.4	-1.7×10^{13}	5.4×10^{12}	1.80	24.7
HfTiON 500 °C	1.68	11.9	-1.4×10^{13}	7.8×10^{12}	2.22	20.9

600 °C indicate unpinned Fermi level¹⁷ and good interface properties. Moreover, the hysteresis voltage is smaller for the HfTiON/TaON samples than the HfTiON samples, especially for the HfTiON/TaON sample annealed at 600 °C (50 mV), as shown in Fig. 1, implying fewer slow states in the dielectric and near/at the interface due to the reduction of Ga and As diffusions in the sample with TaON IPL.¹⁸

The capacitance equivalent thickness (CET), equivalent k value, flatband voltage (V_{fb}) and equivalent oxide-charge density (Q_{ox}) of the samples were extracted from their HF C-V curves, as listed in Table I. Interface-state density (D_{it}) at midgap is also extracted from the C-V curves using the Terman's method for comparison purpose. The CET of the HfTiON/TaON stacked dielectric annealed at 600 °C is 1.65 nm, the smallest among the samples, which is associated with efficiently suppressed growth of the low-k interfacial layer (see Fig. 2). As a result, this sample achieves the largest equivalent k value of 26.2. The positive shift of V_{fb} indicates presence of negative oxide charges in the dielectric film. Smaller positive shift of V_{fb} for the HfTiON/TaON sample annealed at 600 °C (0.93 V) than that annealed at 500 °C (1.19 V) should be attributed to the fact that more incorporated nitrogen atoms can diffuse to fill up the oxygen vacancies in the oxynitride during the higher annealing temperature,¹⁹ resulting in a reduction of defect traps in the film and near the interface. The negative Q_{ox} could be associated with acceptor-like interface and near-interface traps.^{20,21} The Q_{ox} of the HfTiON/TaON sample annealed at 600 °C (9.3×10^{12} cm⁻²) is smaller than that of its counterpart annealed at 500 °C (1.3×10^{13} cm⁻²), probably due to the formation of more-densified high-quality TaON and HfTiON films and better release of near-interface stress during the PDA at higher temperature,²² thus better quality for the HfTiON/TaON and TaON/GaAs interfaces. Moreover, the samples with TaON IPL exhibit smaller D_{it} than those without, with the smallest value for the HfTiON/TaON sample annealed at 600 °C (1.0×10^{12} cm⁻²eV⁻¹). This further indicates the effective blocking role of the TaON interlayer against the diffusions of Hf, Ti, and O towards the GaAs surface during the annealing at higher temperature, as confirmed by the XPS analysis below, thus reducing the defects at/near the interface.²³

Fig. 3 is the gate leakage properties of the samples. High gate leakage current density is observed when a positive gate voltage is applied to the samples without TaON interlayer, with 3.8×10^{-3} A/cm² and 1.4×10^{-2} A/cm² at $V_g = V_{fb} + 1$ V for the samples annealed at 600 °C and 500 °C, respectively. This is likely due to interface trap-assisted tunneling^{24,25} because a high density of interface states exists at the high-k/GaAs interface of the unpassivated

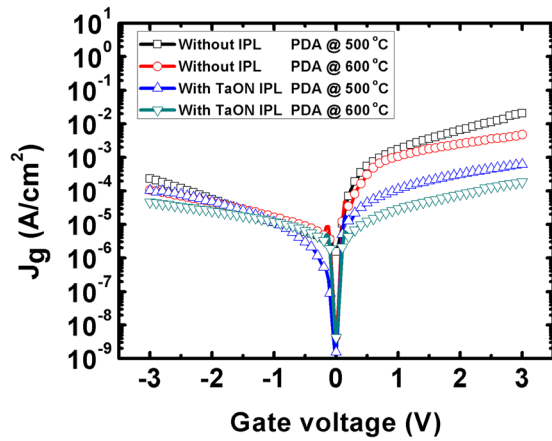


FIG. 3. J_g - V_g characteristics of GaAs MOS capacitors with/without TaON, annealed at 500 and 600 °C.

samples, as listed in Table I. At a moderate or high oxide electric field, the energy levels of some traps in the HfTiON dielectric are lowered to below the Fermi level of the gate, and thus these traps become effective centers for generating the trap-assisted tunneling current.²⁶ The trapped electrons tunnel from the occupied traps to the nearest unoccupied ones and then tunnel to the conduction band of the HfTiON dielectric.²⁷ In addition, the interfacial Ga-/As-oxide induced lowering of the conduction-band offset between HfTiON and GaAs is another possible reason.²⁸ However, a large reduction (nearly two orders of magnitude) of gate leakage current density is obtained for the HfTiON/TaON samples, with 7.3×10^{-5} A/cm² and 3.6×10^{-4} A/cm² for the samples annealed at 600 °C and 500 °C, respectively. The smallest gate leakage current of the HfTiON/TaON sample annealed at 600 °C is closely related to its smallest D_{it} and Q_{ox} . In other words, improved interface properties and reduced defects in the gate oxide can effectively reduce the trap-assisted tunneling current caused by the tunneling of trapped carriers in the sample.²⁵

In order to further identify the effects of the TaON interlayer on the interfacial chemical states, the thickness of the HfTiON layer is reduced by etching to ~ 3 nm from the GaAs surface (as marked in Fig. 2) using an *in situ* Ar⁺ ion beam in the XPS chamber. So, the chemical states near/at the high-k/GaAs interface can be analyzed. The presence of nitrogen is confirmed by the N 1s spectrum, as shown in the inset of Fig. 4(a). In Fig. 4(a), a peak at 22.9 eV should correspond to Ta-N bonds, while the two peaks at 26.1 eV and

28.2 eV come from Ta-O bonds, indicating that a TaON interfacial layer has been formed on the GaAs substrate.

In Fig. 5(a), the intensity of the two Ti 2p peaks is obviously decreased for the sample with TaON interlayer as compared to the one without, suggesting that the Ti content near the GaAs surface is lower in the former. Moreover, the spectra of the HfTiON/TaON sample in Fig. 4(a) reveal a smaller Hf-O peak than that of the HfTiON sample in Fig. 4(b), and, similarly, from Fig. 5(b), it is also found that the O 1s peak is smaller for the former than the latter. Based on the oxygen peak area, thickness of dielectric film and annealing time of the two 600 °C-annealed samples, the ratio of oxygen diffusion rate for the sample with TaON to that without TaON is estimated to be 81%. These imply that TaON can effectively block the Ti, Hf, and O diffusions to the surface of the GaAs substrate and protect it from oxidation, thus reducing the interface states and gate leakage current, as shown in Table I and Fig. 3.

From Figs. 4 and 6, Ga-S and As-S peaks are also observed in the Ga 3d and As 3d spectra of the two 600 °C-annealed samples with or without TaON IPL. This implies that sulfur passivation is beneficial to reducing the formation of Ga-O and As-O bonds,³ but cannot fully eliminate them. In Fig. 4(b), for the sample without TaON interlayer, the Ga-O peak is clearly observed and the content of Ga-O bond at the interface is calculated to be 34% based on the Ga-O/Ga_{3d} peak-area ratio,^{6,13} demonstrating the existence of a significant amount of Ga oxide at the interface. Nevertheless, for the sample with TaON interlayer, no Ga-O peak appears, implying that the formation of Ga oxide at the interface is effectively suppressed by the TaON interlayer. Similarly, As-O bonding only occurs in the HfTiON sample (its content is 2% from the As-O/As_{3d} peak-area ratio) but disappears in the HfTiON/TaON sample, as shown in Fig. 6. Such a low content of As-O bond at the HfTiON/GaAs interface may be due to the decomposition of As oxide into Ga oxide and elemental As ($\text{As}_2\text{O}_3 + \text{GaAs} \rightarrow \text{Ga}_2\text{O}_3 + \text{As}$) during the PDA at 600 °C, which is also the reason for the high content of Ga-O bond at the interface.¹² These indicate that the TaON film as IPL is more effective in suppressing the formation of the Ga-/As-oxides and low-k interfacial layer, thus resulting in good interface properties and large accumulation capacitance, as shown in Fig. 1. Also, it can be observed that the intensity of the As-As peak for the sample with TaON interlayer (a content of 6% from the As-As/As_{3d} peak-area ratio) is lower than that of the sample without TaON IPL

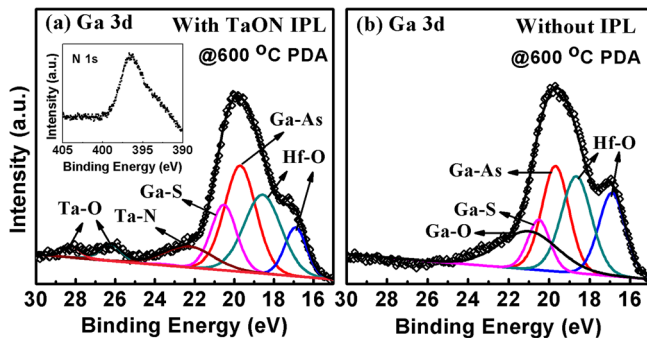


FIG. 4. Ga 3d spectra of the HfTiON/GaAs interface for samples annealed at 600 °C. (a) with TaON and (b) without TaON.

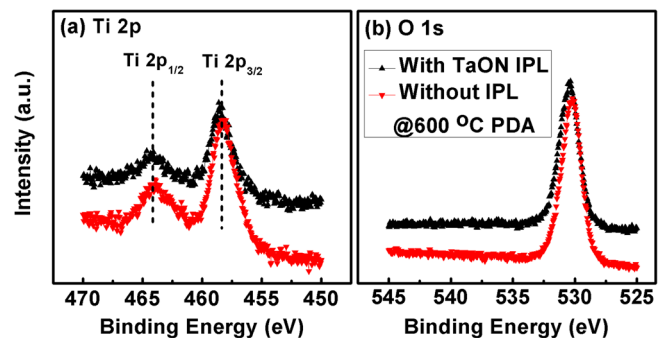


FIG. 5. XPS spectra of the HfTiON/GaAs interface for samples annealed at 600 °C. (a) Ti 2p and (b) O 1s.

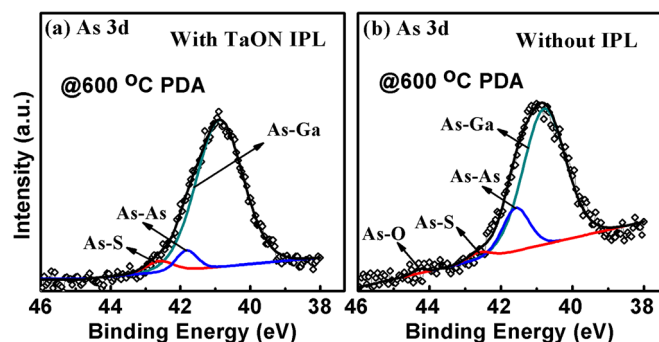


FIG. 6. As 3d spectra of the HfTiON/GaAs interface for samples annealed at 600 °C. (a) with TaON and (b) without TaON.

(a content of 17%). It is well known that a considerable amount of As-O and As-As bonds lead to Fermi-level pinning of the GaAs surface.¹¹ Therefore, all these XPS results show that the TaON IPL on sulfur-passivated GaAs can effectively remove the defective interface bonds and unpin the Fermi level of the GaAs surface, thus greatly improving the interfacial and electrical properties of the devices.

In summary, an ultrathin TaON film has been used to passivate the surface of GaAs substrate, together with $(\text{NH}_4)_2\text{S}$ treatment. The XPS results show that the TaON interlayer formed prior to the deposition of high-k HfTiON gate dielectric can effectively block the diffusions of Hf, Ti, and O towards the GaAs surface and thus suppress the formation of interfacial Ga-/As-oxides and relevant defects, eliminating the Fermi-level pinning at the HfTiON/GaAs interface. As a result, largely improved interface properties and reduced gate leakage current have been achieved for the sulfur-passivated GaAs MOS capacitor with HfTiON/TaON stacked gate dielectric annealed at 600 °C. Therefore, TaON interlayer is a promising surface-passivation technique for making high-performance GaAs-based MOSFETs with high-k gate dielectric.

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